

## Search Forms

## Search Results

## Refine Search

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Search Results -

User Searches

Preferences

Logout

Term	Documents
COMPUTATION\$1	0
COMPUTATION	146259
COMPUTATIONA	7
COMPUTATIONC	1
COMPUTATIONG	1
COMPUTATIONI	3
COMPUTATIONL	3
COMPUTATIONM	1
COMPUTATIONR	3
COMPUTATIONS	42237
COMPUTATIONV	1
(L2 AND (COMPUTATION\$1 OR CALCULATION\$1) ).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	44

There are more results than shown above. [Click here to view the entire set.](#)

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L3 ☐

Refine Search

Recall Text 

Clear

Interrupt

## Search History

DATE: Tuesday, February 17, 2004 [Printable Copy](#) [Create Case](#)

Set  
Name Query  
 side by  
 side

Hit  
Count Set  
Name  
 result  
 set

*DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*

L3 L2 and (computation\$1 or calculation\$1)

44 L3

L2 L1 and (co near1 process\$3 or dsp or digital near1 signal)

56 L2

L1 select\$5 near8 (math or mathematic\$3 or arithmetic\$3 or adder\$1 or multiplier\$1 or multiplication or addition or division\$1 or computation\$3) near9 register\$1 near2 file

185 L1

END OF SEARCH HISTORY

## Refine Search

### Search Results -

Term	Documents
(3 AND 8).PGPB,USPT.	28
(L3 AND L8 ).PGPB,USPT.	28

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L9

Refine Search

Recall Text

Clear

Interrupt

### Search History

 DATE: Tuesday, February 17, 2004    [Printable Copy](#)    [Create Case](#)

Set  
Name Query  
 side by  
 side

Hit    Set  
Count    Name  
              result  
              set

DB=PGPB,USPT; PLUR=YES; OP=OR

L9 13 and L8

28 L9

L8 14 or 15 or 16 or L7

27138 L8

L7 (L5 or L6)! [CCLS]

16234 L7

L6

(708/812 |708/813 |708/814 |708/815 |708/816 |708/817 |708/818 |708/819  
 |708/820 |708/821 |708/822 |708/823 |708/824 |708/825 |708/826 |708/827  
 |708/828 |708/829 |708/830 |708/831 |708/832 |708/833 |708/834 |708/835  
 |708/836 |708/837 |708/838 |708/839 |708/840 |708/841 |708/842 |708/843  
 |708/844 |708/845 |708/846 |708/847 |708/848 |708/849 |708/850 |708/851  
 |708/852 |708/853 |708/854)

2970 L6

(708/101 |708/102 |708/103 |708/104 |708/105 |708/106 |708/107 |708/108  
 |708/109 |708/110 |708/111 |708/112 |708/130 |708/131 |708/132 |708/133  
 |708/134 |708/135 |708/136 |708/137 |708/138 |708/139 |708/140 |708/141  
 |708/142 |708/143 |708/144 |708/145 |708/146 |708/160 |708/161 |708/162

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	708/171	708/172	708/173	708/174	708/190	708/191	708/192	708/200	
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	708/255	708/256	708/270	708/271	708/272	708/273	708/274	708/275	
	708/276	708/277	708/290	708/300	708/301	708/303	708/304	708/305	
	708/306	708/307	708/308	708/309	708/310	708/311	708/312	708/313	
	708/314	708/315	708/316	708/317	708/318	708/319	708/320	708/321	
	708/322	708/323	708/400	708/401	708/402	708/403	708/404	708/405	
	708/406	708/407	708/408	708/409	708/410	708/420	708/421	708/422	
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	708/444	708/445	708/446	708/490	708/491	708/492	708/493	708/494	
<u>L5</u>	708/495	708/496	708/497	708/498	708/499	708/500	708/501	708/502	16093 <u>L5</u>
	708/503	708/504	708/505	708/506	708/507	708/508	708/509	708/510	
	708/511	708/512	708/513	708/514	708/517	708/518	708/519	708/520	
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	708/533	708/534	708/540	708/541	708/542	708/550	708/551	708/552	
	708/553	708/603	708/604	708/605	708/606	708/607	708/620	708/622	
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	708/631	708/632	708/650	708/651	708/652	708/653	708/654	708/655	
	708/656	708/670	708/671	708/672	708/673	708/674	708/675	708/676	
	708/677	708/678	708/679	708/680	708/681	708/682	708/683	708/684	
	708/685	708/700	708/701	708/702	708/703	708/704	708/705	708/706	
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	708/800	708/801	708/802	708/803	708/804	708/805	708/806	708/807	
	708/808	708/809	708/810	708/811)					
<u>L4</u>	(712/2-300)! [CCLS]								9448 <u>L4</u>
	<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>								
	register\$1 near3 file near6 (select\$4) near6 (math or mathematic\$3 or								
<u>L3</u>	computation\$1 or arithmetic\$3) near6 (function\$1 or unit\$1 or block\$1 or								51 <u>L3</u>
	group\$1 or sub near1 unit\$1 or process\$3)								
	sign\$2 near5 (2\$2 or two\$2) near5 complement\$3 and (multiplication\$1 or								
<u>L2</u>	multipl\$5) and normaliz\$7 near15 (divid\$3 or division\$1 or divisor\$1 or								39 <u>L2</u>
	dividend) near20 shift\$3								
	sing\$2 near5 (2\$2 or two\$2) near5 complement\$3 and (multiplication\$1 or								
<u>L1</u>	multipl\$5) and normaliz\$7 near15 (divid\$3 or division\$1 or divisor\$1 or								0 <u>L1</u>
	dividend) near20 shift\$3								

END OF SEARCH HISTORY

## Hit List

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[Generate OACS](#)

Search Results - Record(s) 1 through 20 of 28 returned.

☐ 1. Document ID: US 20020099924 A1

Using default format because multiple data bases are involved.

L9: Entry 1 of 28

File: PGPB

Jul 25, 2002

PGPUB-DOCUMENT-NUMBER: 20020099924

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020099924 A1

TITLE: Processor

PUBLICATION-DATE: July 25, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Nishioka, Kiyokazu	Odawara-shi		JP	
Tanaka, Kazuhiko	Fujisawa-shi		JP	
Fujikawa, Yoshifumi	Yokohama-shi		JP	
Nojiri, Toru	Kawasaki-shi		JP	
Kojima, Keiji	Sagamihara-shi		JP	
Terada, Koichi	Yokohama-shi		JP	
Kurokawa, Yoshiki	Chigasaki-shi		JP	
Hosoki, Koji	Yokohama-shi		JP	

US-CL-CURRENT: 712/24

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. Data
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☐ 2. Document ID: US 20020082714 A1

L9: Entry 2 of 28

File: PGPB

Jun 27, 2002

PGPUB-DOCUMENT-NUMBER: 20020082714

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020082714 A1

TITLE: Processor control apparatus, processor, and processor controlling method

PUBLICATION-DATE: June 27, 2002

INVENTOR-INFORMATION:

h e b b g e e e f e c f e f b e

NAME	CITY	STATE	COUNTRY	RULE-47
Kumamoto, Norichika	Kawasaki		JP	
Tsuruta, Toru	Kawasaki		JP	
Yoshizawa, Hideki	Kawasaki		JP	

US-CL-CURRENT: 700/1; 700/8, 700/9, 712/229

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw De
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☐ 3. Document ID: US 20020029330 A1

L9: Entry 3 of 28

File: PGPB

Mar 7, 2002

PGPUB-DOCUMENT-NUMBER: 20020029330  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020029330 A1

TITLE: Data processing system

PUBLICATION-DATE: March 7, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kamano, Shoichi	Tokyo		JP	
Sugiura, Yoshihide	Tokyo		JP	

US-CL-CURRENT: 712/34

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw De
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☐ 4. Document ID: US 20010011344 A1

L9: Entry 4 of 28

File: PGPB

Aug 2, 2001

PGPUB-DOCUMENT-NUMBER: 20010011344  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20010011344 A1

TITLE: Data processing system and register file

PUBLICATION-DATE: August 2, 2001

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kabuo, Hideyuki	Kyoto-shi		JP	

US-CL-CURRENT: 712/221; 712/244

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw De
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☐ 5. Document ID: US 6601162 B1

L9: Entry 5 of 28

File: USPT

Jul 29, 2003

US-PAT-NO: 6601162

DOCUMENT-IDENTIFIER: US 6601162 B1

TITLE: Processor which executes pipeline processing having a plurality of stages and which has an operand bypass predicting function

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 6. Document ID: US 6401190 B1

L9: Entry 6 of 28

File: USPT

Jun 4, 2002

US-PAT-NO: 6401190

DOCUMENT-IDENTIFIER: US 6401190 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Parallel computing units having special registers storing large bit widths

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 7. Document ID: US 6334135 B1

L9: Entry 7 of 28

File: USPT

Dec 25, 2001

US-PAT-NO: 6334135

DOCUMENT-IDENTIFIER: US 6334135 B1

TITLE: Data processing system and register file

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 8. Document ID: US 6304958 B1

L9: Entry 8 of 28

File: USPT

Oct 16, 2001

US-PAT-NO: 6304958

DOCUMENT-IDENTIFIER: US 6304958 B1

TITLE: Microcomputer having data execution units mounted thereon

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 9. Document ID: US 6282558 B1

L9: Entry 9 of 28

File: USPT

Aug 28, 2001

US-PAT-NO: 6282558

DOCUMENT-IDENTIFIER: US 6282558 B1

TITLE: Data processing system and register file

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 10. Document ID: US 6233678 B1

L9: Entry 10 of 28

File: USPT

May 15, 2001

US-PAT-NO: 6233678

DOCUMENT-IDENTIFIER: US 6233678 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Method and apparatus for profiling of non-instrumented programs and dynamic processing of profile data

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 11. Document ID: US 6128724 A

L9: Entry 11 of 28

File: USPT

Oct 3, 2000

US-PAT-NO: 6128724

DOCUMENT-IDENTIFIER: US 6128724 A

TITLE: Computation using codes for controlling configurable computational circuit

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 12. Document ID: US 6055619 A

L9: Entry 12 of 28

File: USPT

Apr 25, 2000

US-PAT-NO: 6055619

DOCUMENT-IDENTIFIER: US 6055619 A

TITLE: Circuits, system, and methods for processing multiple data streams

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 13. Document ID: US 6047371 A

L9: Entry 13 of 28

File: USPT

Apr 4, 2000

US-PAT-NO: 6047371

DOCUMENT-IDENTIFIER: US 6047371 A

TITLE: Signal processor for performing conditional operation

h e b b g e e f e c f e f b e



Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 14. Document ID: US 5815420 A

L9: Entry 14 of 28

File: USPT

Sep 29, 1998

US-PAT-NO: 5815420

DOCUMENT-IDENTIFIER: US 5815420 A

TITLE: Microprocessor arithmetic logic unit using multiple number representations

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 15. Document ID: US 5682491 A

L9: Entry 15 of 28

File: USPT

Oct 28, 1997

US-PAT-NO: 5682491

DOCUMENT-IDENTIFIER: US 5682491 A

TITLE: Selective processing and routing of results among processors controlled by decoding instructions using mask value derived from instruction tag and processor identifier

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 16. Document ID: US 5590365 A

L9: Entry 16 of 28

File: USPT

Dec 31, 1996

US-PAT-NO: 5590365

DOCUMENT-IDENTIFIER: US 5590365 A

TITLE: Pipeline information processing circuit for floating point operations

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 17. Document ID: US 5574927 A

L9: Entry 17 of 28

File: USPT

Nov 12, 1996

US-PAT-NO: 5574927

DOCUMENT-IDENTIFIER: US 5574927 A

TITLE: RISC architecture computer configured for emulation of the instruction set of a target computer

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 18. Document ID: US 5377335 A

L9: Entry 18 of 28

File: USPT

Dec 27, 1994

US-PAT-NO: 5377335

DOCUMENT-IDENTIFIER: US 5377335 A

TITLE: Multiple alternate path pipelined microsequencer and method for controlling a computer

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 19. Document ID: US 5307300 A

L9: Entry 19 of 28

File: USPT

Apr 26, 1994

US-PAT-NO: 5307300

DOCUMENT-IDENTIFIER: US 5307300 A

TITLE: High speed processing unit

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 20. Document ID: US 5305446 A

L9: Entry 20 of 28

File: USPT

Apr 19, 1994

US-PAT-NO: 5305446

DOCUMENT-IDENTIFIER: US 5305446 A

TITLE: Processing devices with improved addressing capabilities, systems and methods

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs	Generate OACS
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Term	Documents
(3 AND 8).PGPB,USPT.	28
(L3 AND L8).PGPB,USPT.	28

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# Refine Search

Search Results -

Term	Documents
COMPUTATION\$1	0
COMPUTATION	77836
COMPUTATIONA	4
COMPUTATIONL	1
COMPUTATIONS	34993
COMPUTATION1	2
COMPUTATION2	2
COMPUTATION3	1
COMPUTATION+	1
"COMPUTATION%"	1
COMPUTATION:	2
(L13 AND (COMPUTATION\$1 OR CALCULATION\$1)).PGPB,USPT.	58

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Search:

L14

☐

☒

Refine Search

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## Search History

DATE: Tuesday, February 17, 2004   [Printable Copy](#)   [Create Case](#)

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side by side

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*DB=PGPB,USPT; PLUR=YES; OP=OR*

<u>L14</u>	L13 and (computation\$1 or calculation\$1)	58	<u>L14</u>
<u>L13</u>	l12 and (time or cycle\$1 or clock\$1 or period)	101	<u>L13</u>
<u>L12</u>	l10 not l11	102	<u>L12</u>
<u>L11</u>	source near5 dependen\$3 and l10	25	<u>L11</u>
<u>L10</u>	L9 and l2	127	<u>L10</u>
<u>L9</u>	l5 or l6 or l7 or L8	27138	<u>L9</u>
<u>L8</u>	(L6 or L7)![CCLS]	16234	<u>L8</u>
<u>L7</u>	(708/812  708/813  708/814  708/815  708/816  708/817  708/818  708/819	2970	<u>L7</u>
	708/820  708/821  708/822  708/823  708/824  708/825  708/826  708/827		
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	708/234  708/235  708/236  708/250  708/251  708/252  708/253  708/254		
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	708/276  708/277  708/290  708/300  708/301  708/303  708/304  708/305		
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	708/314  708/315  708/316  708/317  708/318  708/319  708/320  708/321		
	708/322  708/323  708/400  708/401  708/402  708/403  708/404  708/405		
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	708/423  708/424  708/425  708/426  708/440  708/441  708/442  708/443		
	708/444  708/445  708/446  708/490  708/491  708/492  708/493  708/494		
	708/495  708/496  708/497  708/498  708/499  708/500  708/501  708/502		
	708/503  708/504  708/505  708/506  708/507  708/508  708/509  708/510		
	708/511  708/512  708/513  708/514  708/517  708/518  708/519  708/520		
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	708/533  708/534  708/540  708/541  708/542  708/550  708/551  708/552		
	708/553  708/603  708/604  708/605  708/606  708/607  708/620  708/622		
	708/623  708/624  708/625  708/626  708/627  708/628  708/629  708/630		
	708/631  708/632  708/650  708/651  708/652  708/653  708/654  708/655		
	708/656  708/670  708/671  708/672  708/673  708/674  708/675  708/676		
	708/677  708/678  708/679  708/680  708/681  708/682  708/683  708/684		
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	708/808  708/809  708/810  708/811)		
<u>L5</u>	(712/2-300 )![CCLS]	9448	<u>L5</u>
<u>L4</u>	(712/2-300 )![CCLS]	35	<u>L4</u>
<u>L3</u>	(712/2-300 )![CCLS]	9448	<u>L3</u>

*DB=USPT; PLUR=YES; OP=OR*

<u>L2</u>	register\$ near1 file near5 select\$3 near5 (math or mathematic\$3 or arithmetic\$3 or add\$3 or multipl\$7)	219	<u>L2</u>
<u>L1</u>	register\$ near1 file near5 select\$3 (math or mathematic\$3 or arithmetic\$3 or add\$3 or multipl\$7)	1755450	<u>L1</u>

END OF SEARCH HISTORY

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L14: Entry 18 of 58

File: USPT

Oct 3, 2000

DOCUMENT-IDENTIFIER: US 6128720 A

TITLE: Distributed processing array with component processors performing customized interpretation of instructions

Brief Summary Text (4):

Three standard techniques used in parallel processing architectures: these include pipelining, use of multiple simple processing elements, and multi-processing. Pipelines are used to achieve time parallelism, where the independent steps in multi-cycle operations are executed in parallel, thereby improving performance. An array of Processing Elements (PEs), termed an array processor, achieves a physical parallelism through operating the multiple elements synchronously in parallel. A multi-processing system achieves an asynchronous parallelism with multiple communicating processes executing on independent systems. This invention is concerned with the pipeline control of multiple processing elements connected together in some topology.

Brief Summary Text (12):

Still further, the customized interpretation of a broadcast instruction by a particular PE can be used by that processor in directing the results of the arithmetic computations to other PEs in the array. Each PE executing an instruction in its customized mode, will drive steering information to steer the results of the computation from that PE to another selected PE in the array.

Detailed Description Text (7):

Turning now to FIG. 2, a more detailed illustration is given of a processor element 120. There it is seen that the processor element 120 includes an instruction buffer 202 which is connected to the instruction bus 110. The instruction buffer 202 is then connected to an instruction register and decode 204. A data buffer 208 is connected to the data bus 112 through the interconnection switch 206. The data buffer 208 is connected to the multiplexer 210. A general purpose register file 212 is connected to the multiplexer 210 and to a selector 214. A plurality of arithmetic units 216 perform various arithmetic functions FN1, FN2, through FNX. The local processor element interconnection switch 206 selectively connects the processor element 120 to various links 205 which connect to other processor 120 in the array 100. A mode register 207 is connected to the instruction register 204 and through the instruction buffer 202 to the instruction bus 110, for storing a topology configuration value from the topology field 302.

Detailed Description Text (8):

Reference can be made to FIG. 5 which shows the instruction pipeline which includes components from the control unit 108 and the processing element 120. Along the left hand margin of FIG. 5 is a vertical line showing the phase stages for a first embodiment of the invention for arrays of processing elements which are 9.times.9 or fewer. Corresponding illustration is shown in FIG. 6 for arrays of processor elements which are greater than 10.times.10. In FIG. 5, it is seen that the phases are divided into a first instruction fetch/distribute phase, followed by a decode phase, followed by an execute and communicate phase which is followed by a condition code return phase. In FIG. 6, it is seen that the phases are divided into a first instruction fetch phase, followed by a distinct distribute phase, which is followed by a decode phase, which is followed by an execute and communicate phase,

which is followed by a condition code phase. The distinct distribute phase shown in FIG. 6 is provided for larger arrays of 10.times.10 processing elements or more, in order to enable additional time to distribute instructions among the various sequencers and processing elements.

Detailed Description Text (19):

FIG. 1 depicts a high level view of the array processor machine organization. The machine organization is partitioned into three main parts: the System Interfaces including Global Memory and external I/O, multiple Control Units with Local Memory, and the Execution Array with Distributed Control PEs. The System Interface is an application-dependent interface through which the array processor interfaces with Global Memory, the I/O, other system processors, and the personal computer/workstation host. Consequently, the System Interface will vary depending upon the application and the overall system design. The Control Units contain the local memory for instruction and data storage, instruction fetch (I-Fetch) mechanisms, and operand or data fetch mechanisms (D-Fetch). The Execution Array with Distributed Control PEs is a computational topology of processing elements chosen for a particular application. For example, the array may consist of N Processing Elements (PEs) per control unit, with each PE containing an Instruction Buffer (IBFR), a General Purpose Register File (GPRF), Functional Execution units (FNS), Communication Facilities (COM), and interfaces to its Instruction/Data buses. The PEs may also contain PE-local instruction and data memories. Further, each PE contains an instruction decode register which supports distributed control of the multiple PEs. Synchronism of local memory accessing is a cooperative process between the control units, local memories, and the PEs. The array of PEs allows computation functions (FNS) to be executed in parallel in the PEs and results to be communicated (COM) between PEs.

Detailed Description Text (21):

FIG. 2 depicts a generalized PE. The PE contains a COM facility identified as the local interconnection switch network. This COM facility provides the means for interfacing the GPRF and the arithmetic elements with neighboring PEs via the Links. The COM facility also provides the connecting interface to the control units local memory subsystem. The general philosophy of the instruction pipeline is for the Control Units, also termed Sequence Processors (SPs), to access instructions and pass on to the PEs any instructions designated to go there. This can be accomplished by use of the tagging of instructions. In a multiple PE organization there is a need to load single and multiple PEs, store register/status registers from single PEs to memory, and control the PEs in different topologies. Rather than proliferate opcodes to accomplish these tasks, tags are created and concatenated to the instructions for PE decode and control. Tags operate as a mode control extension field to the instruction formats. By use of the VLIW concept, the operating modes can be changed on a cycle by cycle basis if required. Since the tag is generated from information stored in a special purpose register, its definition can be machine dependent allowing smaller tags for small machine organizations and larger tags for larger organizations. FIG. 3 depicts a generic form for the tag. The instructions executed by the Processing Elements contain 32 bits plus a system dependent tag field. As an example, the Instruction Tag bits can convey specific status and mode information registered in the SP to the PEs, as well as specific PE identifier values to support individual loading of the PEs. All instructions are defined as broadcast operations going to all PEs associated with a specific control unit's instruction bus. Specific tagged compute instructions are controlled by the tag field. If tagged compute is not specified all PEs execute the instruction independent of the tag-code field.

Detailed Description Text (23):

In many processors, a three-phase fetch, decode, and execute pipeline is used for the basic instruction execution control where the instruction fetched is received in a single instruction decode unit. This requires that an instruction be fetched from one of N instruction memories and then be distributed to N sequencers and PEs

with both the sequencers and PEs decoding and executing in synchronism the received instructions. Depending upon topology size and the intended cycle time, the fetching and distributing of instructions can be accomplished in either a combined fetch/distribute cycle or in separate fetch and distribute cycles. For scalable topologies under consideration of 2.times.2 up to 10.times.10 it is envisioned that a combined fetch/distribute cycle is appropriate. In order to handle relatively high usage arithmetic conditional branch and PE generated exception conditional branch operations, a separate exception condition return phase is provided and two branch execution timings architected. FIG. 4A and FIG. 5 show two views of the four phase pipe; fetch/distribute, decode, execute, and condition code return (See Table 1). Table 1 shows a four phase instruction pipeline diagram example which is depicted in FIG. 5. FIG. 4B and FIG. 6 depict a five phase pipeline for larger topologies with fast cycle times (See Table 2). Table 2 shows a five phase instruction pipeline diagram example which is depicted in FIG. 6.

Detailed Description Text (25):

1. It allows the maximum possible time in the paths from (on-chip) instruction memory to the Sequencer, and from Sequencer to PEs.

Detailed Description Paragraph Table (2):

perform, a forced NOP is generated during this phase. At the end of this phase, the decoded instruction is latched into the SP Execute Register (SXR) and PE Execute Register (PXR). EX/COM Instruction Execute: During this phase, the decoded instructions in the Execute Registers are executed and the results are communicated to the DEST target registers. Note that an instruction will execute in the SP and its associated PEs at the same time. CCR Condition Code Return: A condition code is returned from PEs to the sequencer at the end of the CCR phase.

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Current US Original Classification (1):

712/20

Current US Cross Reference Classification (1):

712/15

Current US Cross Reference Classification (2):

712/209

Current US Cross Reference Classification (3):

712/21

Current US Cross Reference Classification (4):

712/22

Current US Cross Reference Classification (5):

712/226

CLAIMS:

22. The method of claim 20, which further comprises:

said fetching step and said distributing step being performed in a single machine cycle.

23. The method of claim 20, which further comprises:

said fetching step and said distributing step being performed in separate, consecutive machine cycles.



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L11 L10 and co near2 process\$3 493 L11

L10 register near2 file (enabl\$3 or activat\$4) near6 (computation\$3 or arithmetic\$3 or math or mathematic\$3) near4 (function\$1 or block\$1 or element\$1) 13137 L10

L9 L4 near8 (clock\$1 or period\$1 or cycle\$1) and (co near1 process\$3) 180 L9

L8 L4 near12 (clock\$1 or period\$1 or cycle\$1) near30 (co near1 process\$3) 2 L8

L7 L4 near12 (clock\$1 or period\$1 or cycle\$1) near15 (co near1 process\$3) 2 L7

L6 L4 near12 (clock\$1 or period\$1 or cycle\$1) and (co near1 process\$3) 185 L6

L5 L4 near12 (clock\$1 or period\$1 or cycle\$1) 1773 L5

L4 register near2 file (enabl\$3 or activat\$4) near6 (computation\$3 or arithmetic\$3) near4 (unit\$1 or function\$1 or block\$1 or element\$1) 13919 L4

L3 L2 and (computation\$1 or calculation\$1) 44 L3

L2 L1 and (co near1 process\$3 or dsp or digital near1 signal) 56 L2

L1 select\$5 near8 (math or mathematic\$3 or arithmetic\$3 or adder\$1 or multiplier\$1 or multiplication or addition or division\$1 or computation\$3) near9 register\$1 near2 file 185 L1

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L18: Entry 1 of 4

File: USPT

Jun 4, 2002

US-PAT-NO: 6401190

DOCUMENT-IDENTIFIER: US 6401190 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Parallel computing units having special registers storing large bit widths

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 2. Document ID: US 6128724 A

L18: Entry 2 of 4

File: USPT

Oct 3, 2000

US-PAT-NO: 6128724

DOCUMENT-IDENTIFIER: US 6128724 A

TITLE: Computation using codes for controlling configurable computational circuit

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 3. Document ID: US 4882701 A

L18: Entry 3 of 4

File: USPT

Nov 21, 1989

US-PAT-NO: 4882701

DOCUMENT-IDENTIFIER: US 4882701 A

TITLE: Lookahead program loop controller with register and memory for storing number of loop times for branch on count instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 4. Document ID: US 4538223 A

L18: Entry 4 of 4

File: USPT

Aug 27, 1985

US-PAT-NO: 4538223

DOCUMENT-IDENTIFIER: US 4538223 A

TITLE: Computer operand address computation

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachment	Claims	KWIC	Draw De
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